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On: 28 November 2008

By: _____
William S. Francos

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No. : 10/517,471
Applicant(s): Martin Wagner, et al.
Filed: December 7, 2004
TC/A.U.: 2100/2113
Examiner: Bryce P. Bonzo
Atty. Docket: DE 020141
Confirmation No.: 6124
Title: Method and Base Chip for Monitoring the Operation of a Microcontroller Unit

APPEAL BRIEF

Honorable Assistant Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In connection with the Notice of Appeal dated May 7, 2008, and the Notice of Non-compliance dated October 28, 2008, Applicants provide the following Appeal Brief in the above-captioned application.

TABLE OF CASES

1. W.L. Gore & Associates, Inc. v. Garlock, Inc., 220 USPQ 303 (CAFC 1983).
2. In re Paulsen, 30 F.3d 1475, 31 USPQ2d 1671 (Fed. Cir. 1994)
3. In re Spada, 911 F.2d 705, 15 USPQ2d 1655 (Fed. Cir. 1990).
4. Minnesota Min. & Mfg. Co. v. Johnson & Johnson Orthopaedics, Inc., 976 F.2d 1559, 24 USPQ2d 1321 (Fed. Cir. 1992).
5. Scripps Clinic & Res. Found. v. Genentech, Inc., 927 F.2d 1565, 18 USPQ2d 1001 (Fed. Cir. 1991).

1. Real Party in Interest

The owner and assignee of all right, title and interest as evidenced by recordation in the USPTO at Reel/Frame 019719/0843 is NXP Semiconductors, having a principle place of business at High Tech Campus 60, P.O.Box 80073, 5600 KA Eindhoven, The Netherlands.

2. Related Appeals and Interferences

There are no known related appeals or interferences at this time.

3. Status of the Claims

Claims 1 and 3-9 are pending in the present application. Claims 2 and 10 have been cancelled. Claims 1 and 3-9 have been finally rejected. The claims on appeal, claims 1 and 3-9, are duplicated in the Appendix.

4. Status of Amendments

A Final Office Action on the merits was mailed on February 7, 2008. A Notice of Appeal was filed on May 7, 2008. There are no pending amendments.

5. Summary of the Claimed Subject Matter[1]

Referring to claim 1:

In one embodiment, a method of monitoring the operation of at least one microcontroller unit (300) associated with a system (100) comprises: associating at least one monitoring module (10) with the microcontroller unit (300); resetting of the microcontroller unit; and acknowledging the resetting to the monitoring module (10) by transmitting at least one confirming signal. The confirming signal is formed by at least one trigger signal or trigger code that differs from the normal operation of the microcontroller unit or is permitted only once by the monitoring module, or both.

1 In the description to follow, citations to various reference numerals, drawings and corresponding text in the specification are provided solely to comply with Patent Office Rules. It is emphasized that these reference numerals, drawings and text are representative in nature, and in not any way limiting of the true scope of the claims. It would therefore be improper to import any meaning into any of the claims simply on the basis of illustrative language that is provided here only under obligation to satisfy Patent Office rules for maintaining an Appeal.

(Kindly refer to claim 1; Fig. 1 and page 3, line 26 through page 5, line 3 of the filed application).

Referring to claim 4:

In another embodiment, a base chip (200) adapted to monitor operation of at least one microcontroller unit (300). The base chip comprises at least one reset unit (40) connected (42) to the microcontroller unit (300), and adapted to reset the microcontroller unit (300), and at least one monitoring module (10) that is associated with the microcontroller unit (300) and to which the fact that a reset of the microcontroller unit (300) has taken place can be acknowledged by at least one confirming signal wherein the confirming signal is formed by at least one trigger signal or trigger code that differs from the normal operation of the microcontroller unit or is permitted only once by the monitoring module, or both. (Kindly refer to claim 4; Fig. 1 and page 3, line 26 through page 5, line 3 of the filed application application).

6. Grounds of Rejection to be Reviewed on Appeal

The issues in the present matter are whether:

I. Claims 1, 3-6, 8 and 9 were properly rejected under 35 U.S.C. § 102(b) as being anticipated by *Sheldon, et al.* (U.S Patent 6,307,480); and 2

II. Claim 7 was properly rejected under 35 U.S.C. § 103(a) as being obvious in view of *Sheldon, et al.*

7. Argument

In this portion of the Appeal Brief, arguments are provided

At the outset Applicants rely at least on the following standards with regard to proper rejections under 35 U.S.C. § 102. Notably, a proper rejection of a claim under 35 U.S.C. § 102 requires that a single prior art reference disclose each element of the claim. *See, e.g., W.L. Gore & Assoc., Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303, 313

(Fed. Cir. 1983). Anticipation requires that each and every element of the claimed invention be disclosed in a single prior art reference. *See, e.g., In re Paulsen*, 30 F.3d 1475, 31 USPQ2d 1671 (Fed. Cir. 1994); *In re Spada*, 911 F.2d 705, 15 USPQ2d 1655 (Fed. Cir. 1990). Alternatively, anticipation requires that each and every element of the claimed invention be embodied in a single prior art device or practice. *See, e.g., Minnesota Min. & Mfg. Co. v. Johnson & Johnson Orthopaedics, Inc.*, 976 F.2d 1559, 24 USPQ2d 1321 (Fed. Cir. 1992). For anticipation, there must be no difference between the claimed invention and the reference disclosure, as viewed by a person of ordinary skill in the field of the invention. *See, e.g., Scripps Clinic & Res. Found. v. Genentech, Inc.*, 927 F.2d 1565, 18 USPQ2d 1001 (Fed. Cir. 1991).

I. Rejection of claims 1, 3-6

Sheldon, et al. fails to disclose at least one feature of claim 1 and claim 4

Claim 4 is drawn to a base chip adapted to monitor operation of at least one microcontroller unit and features:

"*at least one reset unit connected to the microcontroller unit, and adapted to reset the microcontroller unit, and at least one monitoring module that is associated with the microcontroller unit and to which the fact that a reset of the microcontroller unit has taken place can be acknowledged by at least one confirming signal wherein the confirming signal is formed by at least one trigger signal or trigger code that differs from the normal operation of the microcontroller unit or is permitted only once by the monitoring module, or both.*"

Claim 1 is drawn to a method and includes similar features.

As such, as amended, claims 1 and 4 feature that the *confirming signal is formed by at least one trigger signal or trigger code that differs from the normal operation of the microcontroller unit or is permitted only once by the monitoring module, or both.* In the Office Action, the Examiner directs Applicants to column 4, lines 34-44 of *Sheldon, et al.* for the alleged disclosure of these features. Applicants have reviewed the noted portion

of the reference and respectfully submit that these features are not disclosed therein. Specifically, column 4, lines 34-44 discloses:

> If the battery monitor 20 is generating a low dead battery signal 28, current will flow from V_{cc} through R_P and through the parallel combination of R_{S2} and R_L. The value of R_{S2} is chosen to assure that the resistor divider created by R_P and the parallel combination of R_{S2} and R_L causes a low reset signal 44, indicating that a reset is requested. Further, the value of C_L is chosen such that the time constant of the discharge of C_L is smaller than the duration of the time out signal 26 to assure that the reset signal 44 will arrive at a low level before MN2 is turned off.

The sequence described relates to the request for a reset and receipt of the reset signal before a FET (MN2) is turned off. There is no description of a *confirming signal is formed by at least one trigger signal or trigger code that differs from the normal operation of the microcontroller unit or is permitted only once by the monitoring module, or both.*

For at least the reasons set forth above, the applied art fails to disclose at least one feature of each of claims 1 and 4. Therefore these claims are patentable over the applied art. Moreover, claims 3 and 5-9, which depend from claims 1 and 4, respectively, are also patentable for at least the same reasons.

II. Rejection of claim 7

Applicants submit that claim 7 is patentable at least because of its dependence on claim 4. This notwithstanding, Applicants respectfully submit that the rejection is improper for at least the following reasons. Notably, the Examiner takes Official Notice that it is notoriously well-known to implement a low power fail-safe mode in devices that are not able to reset properly. Yet, the Examiner provides no evidence for this assertion.

As is known, a claim rejection must be based on objective evidence of record, and cannot be supported merely on subjective belief and unknown authority. See, e.g., M.P.E.P. § 2144.03; In re Lee, 277 F.3d at 1344-45, 61 USPQ2d at 1434-35 (Fed. Cir. 2002); In re Zerko, 258 F.3d at 1386, 59 USPQ2d at 1697.

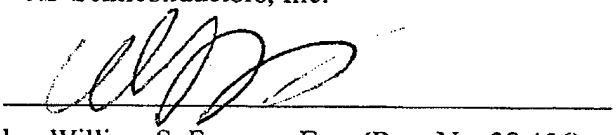
No such concrete evidence has been provided by the Examiner here, nor did the Examiner submit an affidavit as required by 37 C.F.R. § 1.104(d)(2) if this proposed

motive were based on facts within his personal knowledge (see M.P.E.P. § 2144.03). Applicants respectfully request that such an affidavit be provided if a rejection continues to be made without a citation of any objective evidence.

8. Conclusion

In view of the foregoing, applicant(s) respectfully request(s): the withdrawal of all objections and rejections of record; the allowance of all the pending claims; and the holding of the application in condition for allowance.

Respectfully submitted on behalf of:
NXP Semiconductors, Inc.



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Appendix

Claims on Appeal

Claims on Appeal:

1. A method of monitoring the operation of at least one microcontroller unit associated with a system, the method comprising:

associating at least one monitoring module with the microcontroller unit ;

resetting of the microcontroller unit; and

acknowledging the resetting to the monitoring module by transmitting at least one confirming signal, wherein the confirming signal is formed by at least one trigger signal or trigger code that differs from the normal operation of the microcontroller unit or is permitted only once by the monitoring module, or both.

3. A method as claimed in claim 1 wherein, in relation to the operation of the microcontroller unit , a distinction is made between different reset events and in that these different reset events are acknowledged to the monitoring module by means of different confirming signals.

4. A base chip adapted to monitor operation of at least one microcontroller unit the base chip comprising:

at least one reset unit connected to the microcontroller unit , and adapted to reset the microcontroller unit , and at least one monitoring module that is associated with the microcontroller unit and to which the fact that a reset of the microcontroller unit has taken place can be acknowledged by at least one confirming signal wherein the confirming signal is formed by at least one trigger signal or trigger code that differs from the normal operation of the microcontroller unit or is permitted only once by the monitoring module, or both.

5. A base chip as claimed in claim 4, wherein at least one information unit is provided to allow for different reset events, and at least one supply unit is connected to the microcontroller unit .

6. A base chip as claimed in claim 4 , whereinthe monitoring module is adapted to betriggered by at least one interface unit or to distinguish between individual accesses to the monitoring module different reset events can be marked by different trigger values, or both.

7. A base chip as claimed in claim 4 , wherein the base chip is adapted to entera fail-safe mode if the resetting of the microcontroller unit is not acknowledged once by the confirming signal, or if the base chip receives the confirming signal without a reset having taken place previously, there being, in the fail-safe mode, a current consumption that is lower than in normal operation.

8. A base chip as claimed in claim 4 , wherein at least one signal line is provided between the monitoring module and the microcontroller unit , the signal line operative to transmitthe confirming signal, the confirming signal including a trigger signal or a trigger code that differs from a normal operation of the microcontroller unit.

9. A control system comprising at least one microcontroller unit and at least one base chip as claimed claim 4.

Appendix
Evidence (None)

Appendix
Related Proceedings (None)